Remarks

Claims 1-15 remain in the application.

The Abstract of the Disclosure has been amended to eliminate reference numerals.

Claims 1-15 have been amended to eliminate reference numerals, the term "preferably," multiple dependencies, and claiming features in the alternative.

Claims 1-15 have been clarified by amendment above for purposes of form. It is respectfully submitted that the amendments to claims 1-15 are neither narrowing nor made for substantial reasons related to patentablity as defined by the Court of Appeals for the Federal Circuit (CAFC) in Festo Corporation v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd., 95-1066 (Fed. Cir. 2000). Therefore, the amendments to claims 1-15 do not create prosecution history estoppel and, as such, the doctrine of equivalents is available for all of the elements of claim 1-15.

Consideration and allowance of the claims is respectfully requested.

Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version With Markings to Show Changes Made."

5/30/01
Date

Respectfully submitted,

Paul D. Greeley

Paul D. Greeley
Attorney for Applicant(s)
Registration No. 31,019
Ohlandt, Greeley, Ruggiero & Perle, L.L.P.
One Landmark Square, 10th Floor
Stamford, CT 06901-2682
(203) 327-4500

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Specification

On page 32, line 1, replace "ABSTRACT" with --ABSTRACT OF THE DISCLOSURE--.

In The Abstract of the Disclosure

Please amend the Abstract of the Disclosure as follows:

[Disclosed is an a] Automated test equipment [–] (ATE) [- (200) having] includes a tester-per-pin architecture with a [plurality] number of individual decentralized per-pin testing units [(700)], wherein each per-pin testing unit [(700i) being] is adapted for testing a respective DUT-pin [(di)] of a device under test [–] (DUT) [- (600)] by emitting stimulus response signals to the respective DUT-pin and/or receiving stimulus response signals from the respective DUT-pin. [For t] Testing the DUT, [the following steps are executed:] includes defining [–] for a testing sequence [-] the DUT into one or more DUT-cores representing one or more functional units of the DUT and covering one or more DUT-pins of the DUT, and assigning [-] during the testing sequence [-] one or more of the per-pin testing units [(700i)] to one or more ATE-ports [(210-240)], whereby each ATE-port comprises one or more of the per-pin testing units [(700i)] and represents an independent functional testing unit for testing one or more of the DUT-cores during the testing sequence.

[[Fig. 2 for publication]]

In The Claims

Please amend the claims as follows:

1. (Amended) An automated test equipment [–] (ATE) [- (200) having] comprising:

a tester-per-pin architecture [with] having a plurality of individual decentralized per-pin testing units [(700)], wherein each per-pin testing unit [(700i) being] is adapted for testing a respective [DUT-] pin [(di)] of a device under test [–] (DUT) [- (600)] by at least

one of emitting stimulus response signals to [the] said respective DUT-pin and [/or] receiving stimulus response signals from [the] said respective DUT-pin, wherein [-] during a testing sequence, [-] the DUT [(600)] is defined [into] as one or more DUT-cores representing one or more functional units of [the] said DUT [(600)] and [covering] including one or more DUT-pins of [the] said DUT [(600)]; and

means for assigning, [-] during [the] said testing sequence, [-] one or more of [the] said per-pin testing units [(700i)] to one or more ATE-ports [(210-240)], whereby each ATE-port comprises one or more of [the] said per-pin testing units [(700i)] and represents an independent functional testing unit for testing one or more of [the] said DUT-cores during [the] said testing sequence.

2. (Amended) The automated test equipment [(200)] of claim 1, wherein [the] said means for assigning comprises:

switching means for switching connections between one or more of [the] said per-pin testing units [(700i)] and one or more of [the] said DUT-pins, and

controlling means for controlling the switching of [the] said switching means in accordance with the assigning of [the] said one or more of the per-pin testing units [(700i)] to [the] said one or more ATE-ports [(210-240)] during [the] said testing sequence.

3. (Amended) The automated test equipment [(200)] of claim 1, wherein at least one of [the] said ATE-ports [(210-240)] comprises programming means for independently defining [and/or] at least one of programming timing and[/or] a stimulus/response pattern[, as if the set of DUT-pins assigned to the one ATE-port constituted a device in itself].

4. (Amended) The automated test equipment [(200)] of claim 3, wherein [the] said programming means comprises at least one of:

means for specifying cycle times of stimulus and response vectors for [the] said at least one ATE-port; [and/or]

means for specifying a per-pin timing in terms of sets of available waveforms for each

ATE-pin of the one ATE-port, whereby each waveform represents a sequence of events of various types occurring at specified instances in time; [and/or]

means for specifying a pattern program for the one ATE-port; [and/or]

means for specifying a per-pin vector data for each pin of the one ATE-port; and[/or]

means for specifying analogue set-up conditions for analogue pins of the one ATE-port.

5. (Amended) The automated test equipment [(200)] of claim 3 [or 4], wherein [the] said programming means comprises:

main pattern programs for implementing access protocols to one or more of [the] said DUT-cores through a shared set of per-pin testing units [(700i) constituting] comprising one individual ATE-port comprising at least [the] per-pin testing units [(700i)] that are part of the ATE-ports utilized to access [the] said one or more [of the] DUT-cores, and

independent pattern programs for implementing stimulus and response patterns for each DUT-core of [the] said one or more [of the] DUT-cores.

6. (Amended) The automated test equipment [(200)] of claim 5, wherein [the] said main pattern program comprises at least one of:

means for configuring [the] said one individual ATE-port for activating [the] said per-pin testing units [(700i)] thereof for accessing [the] said one or more [of the] DUT-cores [to be accessed]; and[/or]

means for selecting pattern data generated by [the] pattern programs of [the] said accessed [one or more of the] DUT-cores during one testing sequence for testing [the one or more of the] said accessed DUT-cores [to be accessed].

7. (Amended) The automated test equipment [(200)] of claim 3, wherein [the] said programming means comprises:

specifying means for specifying an alias mapping between per-pin testing units [(700i)] for a plurality of [the] said ATE-ports, [preferably] for specifying at least one of timing

information[,] and a pattern program[, or other test condition sets] of one individual ATE-port to apply for the plurality of the ATE-ports for which the alias mapping is defined.

8. (Amended) The automated test equipment [(200)] according to claim 1, further comprising specifying means for specifying overall test conditions for a test that concurrently operates on multiple ATE-ports.

9. (Amended) The automated test equipment [(200)] of claim 8, wherein the specifying means comprises at least one of:

means for determining a set of concurrently active ATE-ports during a defined testing sequence; [and/or]

means for selecting the ATE-port test conditions for one or more ATE-pins, [preferably] for selecting an ATE-port timing setup for one or more ATE-pins; [and/or]

means for specifying global test conditions to express dependencies between pins of the DUT and the ATE[, preferably global DUT specifications]; and[/or]

means for determining a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port.

10. (Amended) A method for testing a device under test [–] (DUT) [- (600)] with [an] automated test equipment [–] (ATE) [- (200) having] comprising a tester-per-pin architecture [with] having a plurality of individual decentralized per-pin testing units [(700)], wherein each per-pin testing unit [(700i) being] is adapted for testing a respective [DUT-]pin [(di)] of [the] said DUT [(600)] by at least one of emitting stimulus response signals to [the] said respective DUT-pin and [/or] receiving stimulus response signals from [the] said respective DUT-pin, [the] said method comprising [the steps of]:

[(a)] defining [–] for a testing sequence [- the] said DUT [(600) into] as one or more DUT-cores representing one or more functional units of [the] said DUT [(600)] and [covering] including one or more [DUT-]pins of [the] said DUT [(600)], and:

[(b)] assigning [-] during [the] said testing sequence [-] one or more of [the]

said per-pin testing units [(700i)] to one or more ATE-ports [(210-240)], whereby each ATE-port comprises one or more of [the] said per-pin testing units [(700i)] and represents an independent functional testing unit for testing one or more of [the] said DUT-cores during [the] said testing sequence.

11. (Amended) The method of claim 10, further comprising [the step of]:

[(c)] defining [and/or] at least one of programming timing and[/or] a stimulus/response pattern for one or more of [the] said ATE-ports [(210-240), as if the set of DUT-pins assigned to one of the ATE-ports constituted a device in itself].

12. (Amended) The method of claim 11, wherein [step (c)] defining at least one of programming timing and a stimulus/response pattern comprises [one or more of the steps] at least one of:

[(c1)] specifying cycle times of stimulus and response vectors for the one ATE-port;

[(c2)] specifying a per-pin timing in terms of sets of available waveforms for each per-pin testing unit [(700i)] of the one ATE-port, whereby each waveform represents a sequence of events of various types occurring at specified instances in time;

[(c3)] specifying a pattern program for the one ATE-port, preferably specifying common sequencing instructions for all per-pin testing units [(700i)] of the one ATE-port;

[(c4)] specifying per-pin vector data for each per-pin testing unit [(700i)] of the one ATE-port; and

[(c5) means for] specifying analogue set-up conditions for analogue pins of the one ATE-port.

13. (Amended) The method according to [any one of the claims 9] claim 11,

further comprising [a step of]:

[(d)] specifying overall test conditions for a test that concurrently operates on multiple ATE-ports.

14. (Amended) The method of claim 13, wherein [step (d)] specifying overall test conditions comprises [one or more of the steps]:

[(d1)] determining a set of concurrently active ATE-ports during a defined testing sequence;

[(d2)] selecting the ATE-port test conditions for one or more ATE-pins, preferably for selecting an ATE-port timing setup for one or more ATE-pins;

[(d3)] specifying global test conditions to express dependencies between pins of the DUT and the ATE, preferably global DUT specifications; and

[(d4)] determining a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port.

15. (Amended) [A software program or product, preferably stored on a] A data [carrier, for executing the method according to claim 10, when run on a data processing system such as a computer] media comprising:

a means for testing a device under test (DUT) with automated test equipment (ATE) comprising a tester-per-pin architecture having a plurality of individual decentralized per-pin testing units, wherein each per-pin testing unit is adapted for testing a respective pin of said DUT by at least one of emitting stimulus response signals to said respective DUT-pin and receiving stimulus response signals from said respective DUT-pin;

means for defining for a testing sequence said DUT as one or more DUT-cores representing one or more functional units of said DUT and including one or more pins of said DUT; and

means for assigning during said testing sequence, one or more of said per-pin

testing units to one or more ATE-ports, whereby each ATE-port comprises one or more of said per-pin testing units and represents an independent functional testing unit for testing one or more of said DUT-cores during said testing sequence.